REMARKS

The application has been reviewed in light of the final Office Action dated August 28, 2007. Claims 1-21 were pending. By this Amendment, claims 1-18 and 21 have been canceled, without prejudice or disclaimer, claim 19 has been amended to clarify the claimed subject matter, and new claims 22-38 have been added. Accordingly, claims 19, 20 and 22-38 are now pending, with claims 19, 22 and 31 being in independent form.

Claims 1 and 10 were rejected under 35 U.S.C. § 102(b) as purportedly anticipated by U.S. Patent No. 5,758,191 to Kasebayashi et al. Claims 2, 3, 9, 11, 12, 18 and 21 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi in view of U.S. Patent No. 6,799,242 to Tsuda et al. Claims 4-6 and 13-15 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi in view of Tsuda and further in view of U.S. Patent No. 6,470,439 to Yamada et al. Claims 7, 8, 16 and 17 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi in view of Tsuda and Yamada and further in view of U.S. Patent No. 6,502,159 to Chuang. Claims 19 and 20 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi in view of Tsuda and further in view of U.S. Patent No. 6,631,469 to Silvester.

Applicant respectfully submits that independent claims 19, 22 and 31 are patentable over the cited art, for at least the following reasons.

The present application relates to various improvements devised by applicant for data transfer between an optical disk drive apparatus with a host computer.

For example, claim 19 is directed an optical disk drive apparatus comprising an optical disk drive mechanism and an interface circuit. The interface circuit interfaces communications between the optical disk drive mechanism and a host computer, and comprises an input terminal

for receiving data sent from the host computer, a data processor, a clock generator, an operation mode changer and a buffering circuit block configured to buffer the data received through the input terminal. The clock generator generates a clock signal with which the data processor performs a predetermined data processing operation to the data received through the input terminal. The operation mode changer controls the clock generator to reduce a frequency of the clock signal to a value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode.

As another example, claim 22 is directed to an optical disk drive apparatus comprising (a) an optical disk drive mechanism, (b) a register circuit including a plurality of registers which store data to be transferred from the optical disk drive apparatus to a host computer, (c) a first memory which stores first information indicating specific addresses of corresponding specified registers in the register circuit and representing an access executed by the host computer to the optical disk drive mechanism for a data transfer, (d) a second memory which stores second information, sent in association with the first information stored in the first memory and corresponding to said data to be transferred from the optical disk drive apparatus to said host computer, to be written into the specified registers of the register circuit at the specific addresses indicated by the first information stored in the first memory, and (e) a control circuit configured to perform an information writing operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed, in connection with said data to be transferred from the optical disk drive apparatus to said host computer.

Kasebayashi, as understood by Applicant, proposes a magnetic disk drive apparatus including a buffer 11 having an area for storing burst data and another area for storing data in

connection with write and read commands.

Kasebayashi, as acknowledged in the Office Action, does not teach or suggest an optical disk drive apparatus comprising an optical disk drive mechanism.

Independent claim 19

In addition, Kasebayashi, as also acknowledged in the Office Action, does not teach or suggest an apparatus including a clock generator which generates a clock signal with which a data processor performs a predetermined data processing operation to data received through an input terminal, and an operation mode changer which controls the clock generator to reduce a frequency of the clock signal to a value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode.

Tsuda does not cure all of the deficiencies of Kasebayashi, with respect to claim 19 of the present application.

Tsuda, as understood by Applicant, proposes an optical disc player apparatus that enters a sleep mode when it is inactive for a predetermined time.

Tsuda, column 7, line 57 through column 8, line 10, which was cited in the Office Action, states as follows:

> Entry into the sleep mode will now be described. When a sleep command is issued from the host computer to the host interface 13, it is transferred via the microcomputer interface 233 to the control microcomputer 244, which responds by delivering a TOC transfer command to the memory control circuit 232 via the microcomputer interface 233. On the basis of the first address and the size data stored in the address register 230, the memory control circuit 232 reads the TOC data from the buffer RAM 7, and transfers it to the microcomputer interface 233, where a part of the TOC data is temporarily stored in a register (not shown). The memory control circuit 61 reads the TOC data stored in the register of the microcomputer interface 233, and writes it to the SRAM 56 in a sequential manner beginning with the first address. A succeeding portion of the TOC data continues to be written to a storage region of the SDRAM 56 for which the write operation has been completed. After the write operation of the TOC data into the SDRAM 56 is completed, ***the control microcomputer 244 delivers a stop command to the clock generator circuit 62,***

which then stops generating the clock signal, thus entering the sleep mode

Thus, in the apparatus proposed by Tsuda, **no clock signals are generated in sleep mode**.

Accordingly, Tsuda, contrary to the contention in the Office Action, does not teach or suggest an apparatus including an operation mode changer which controls the clock generator to ***reduce a frequency of the clock signal to a value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode***, as provided by the subject matter of claim 19 of the present application.

Further, the Office Action equates analog signal processor 4 and digital signal processor 5 in Fig. 1 of Tsuda with the data processor of claim 19 of the present application. However, Tsuda, column 7, line 57 through column 8, line 10 describes entry into sleep mode in the optical disc player apparatus shown in Fig. 7 of Tsuda, and Fig. 1 of Tsuda shows a conventional optical disc player apparatus wherein generation of reference clock signals cannot cease in sleep mode since they are required for refresh operations (see Tsuda, column 3, lines 17-19). Thus, contrary to the contention in the Office Action, the clock signal generation and cessation as proposed at column 7, line 57 through column 8, line 10 cannot control the processing operation of the analog signal processor 4 and digital signal processor 5 in Fig. 1 of Tsuda.

In addition, Kasebayashi and Tsuda, as implicitly acknowledged in the Office Action, does not teach or suggest a buffering circuit block configured to buffer the data received through an input terminal of the optical disk drive apparatus from the host computer, the buffering circuit block including a first data transfer path, a second data transfer path and a path selection controller, wherein the first data transfer path is configured to transfer the data received through the input terminal to the data processor not via a memory, the second data transfer path is

configured to transfer the data received through the input terminal to the data processor via a memory, and the path selection controller controls the buffering circuit block to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode, as provided by the subject matter of claim 19 of the present application.

Silvester does not cure the deficiencies of Kasebayashi and Tsuda.

Silvester, as understood by Applicant, proposes a computer system having a sleep mode, and in the sleep mode, a wakeup alarm is triggered in the computer system according to a user-specified periodic interval, and in response to the wakeup alarm, the computer system automatically exits the sleep mode and enters a wake mode, and then automatically exchanges data, such as email, with a host and thereafter returns to the sleep mode.

Processor 100, communication device 120, hard drive 125 and communication device 130 of Silvester are equated in the Office Action with the buffering circuit block of claim 19 of the present application.

However, the processor 100, communication device 120, hard drive 125 and communication device 130 of Silvester do not buffer the data received through an input terminal of the optical disk drive apparatus from the host computer.

Therefore, the combination of Silvester, Kasebayashi and Tsuda fails to disclose or suggest an optical disk drive apparatus wherein an operation mode changer controls a clock generator to reduce a frequency of the clock signal to a value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode, and wherein a buffering circuit block buffers the data received through an input terminal of the optical disk drive apparatus from the host computer, the buffering circuit block including a first

data transfer path, a second data transfer path and a path selection controller, wherein the first data transfer path is configured to transfer the data received through the input terminal to the data processor not via a memory, the second data transfer path is configured to transfer the data received through the input terminal to the data processor via a memory, and the path selection controller controls the buffering circuit block to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode, as provided by the subject matter of claim 19 of the present application.

Further, it is submitted that it would not have been obvious to combine Kasebayashi and/or Silvester with Tsuda. As previously pointed out, Kasebayashi relates to a magnetic disk drive apparatus. While a system can include both a magnetic disk drive apparatus and an optical disk drive apparatus, it would not have been obvious to modify the optical disk player apparatus of Tsuda based on the features of the magnetic disk drive apparatus of Kasebayashi. Likewise, it would not have been obvious to modify the optical disk player apparatus of Tsuda based on the features of the computer proposed by Silvester.

Accordingly, Applicant respectfully submits that independent claim 19 and claims depending therefrom are patentable over the cited art.

Independent claims 22 and 31

As mentioned above, claim 22 of the present application is directed to an optical disk drive apparatus comprising an optical disk drive mechanism, and Kasebayashi, as acknowledged in the Office Action, does not teach or suggest an optical disk drive apparatus comprising an optical disk drive mechanism.

As also pointed out above, while a system can include both a magnetic disk drive

apparatus and an optical disk drive apparatus, it would not have been obvious to modify the optical disk player apparatus of Tsuda based on the features of the magnetic disk drive apparatus of Kasebayashi.

Further, as previously pointed out in the record, Kasebayashi, contrary to the position taken by the Examiner, does not teach or suggest an apparatus comprising a second memory which ***stores second information, sent in association with the first information (indicating a specific address of a register circuit) stored in the first memory and corresponding to data to be transferred to a host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory***.

The Office Action (page 15) states as follows:

> Regarding Claims 1 and 10, Applicant argues that "the read unit 14 in the system proposed by Kasebayashi, contrary to the contention in the Office Action, does not store data from the magnetic disk 13", and further "[i]t can be seen clearly in Fig. 3 of Kasebayashi that the data from the magnetic disk 13 flows directly to the buffer 11." The examiner respectfully disagrees. Contrary to Applicant's argument, Kasebayashi does in fact teach this limitation. In Column 5, lines 57-61 of Kasebayashi, it is stated that "read unit 14 ... reads data required by the host system 10 from the magnetic disk 13, and writes the data in the read/write area indicated by the address information." The term "read", as defined by the Microsoft Computer Dictionary, Fifth Edition (attached), is "[t]he action of transferring data from an input source into a computer's memory" (see definition [1]). Therefore, it can be seen that read unit 14 does in fact store data from the magnetic disk 13.

Even assuming *arguendo* that the definition of the term "read" from the Microsoft Computer Dictionary is apropos here (which applicant does not concede), the "read" operation to which Kasebayashi refers to reading the data into the memory of **host computer system 10**.

Such construction of the term read as used in Kasebayashi is consistent with Fig. 3 of Kasebayashi which is reproduced below:

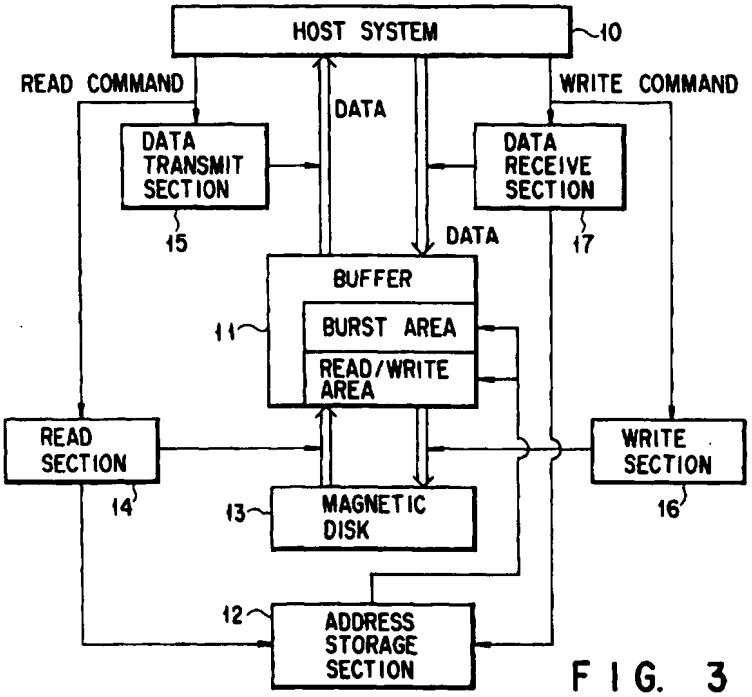

FIG. 3

Fig. 3 of Kasebayashi clearly show that the data from the magnetic disk 13 flows directly to the buffer 11. There are no arrows indicating flow of data from the magnetic disk 13 to the read section 14. On the other hand, the read unit 14 does control flow of the data from the magnetic disk 13 directly to the buffer 11.

Thus, one skilled in the art would not have construed Kasebayashi as suggesting that the read section 14 has an internal memory, and one skilled in the art would have understood Kasebayashi as proposing that the data flows directly from the magnetic disk 13 to the buffer 11, under control of the read section 14.

Further, as previously pointed out in the record, the address storage unit 12 of Kasebayashi does not store specific addresses corresponding to the data to be transferred to the

host computer (that is, with each address indicating a buffer location into which a corresponding data is to be written).

Kasebayashi simply does not teach or suggest an optical disk drive apparatus comprising a communications interface apparatus comprising a register circuit, a first memory, a second memory and a control circuit, wherein the register circuit includes a plurality of registers which store data to be transferred from the optical disk drive apparatus to a host computer, the first memory stores first information indicating specific addresses of corresponding specified registers in the register circuit, and the second memory stores second information, sent in association with the first information stored in the first memory and corresponding to said data to be transferred to said host computer, to be written into the specified addresses of the register circuit at the specific addresses indicated by the first information stored in the first memory, as provided by the subject matter of claim 22 of the present application.

The other cited references, as discussed in the record, do not cure the above-mentioned deficiencies of Kasebayashi.

Applicant simply does not find teaching or suggestion in the cited art of an optical disk drive apparatus comprising a communications interface apparatus comprising a register circuit, a first memory, a second memory and a control circuit, wherein the register circuit includes a plurality of registers which store data to be transferred from the optical disk drive apparatus to a host computer, the first memory stores first information indicating specific addresses of corresponding specified registers in the register circuit, and the second memory stores second information, sent in association with the first information stored in the first memory and corresponding to said data to be transferred to said host computer, to be written into the specified addresses of the register circuit at the specific addresses indicated by the first information stored

in the first memory, as provided by the subject matter of claim 22 of the present application.

Independent claim 31 is patentably distinct from the cited art for at least similar reasons.

Accordingly, Applicant respectfully submits that independent claims 22 and 31, and the claims depending therefrom, are patentable over the cited art.

In view of the remarks hereinabove, Applicant submits that the application is now in condition for allowance. Accordingly, Applicant earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Patent Office is hereby authorized to charge any fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,

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